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TITLE: Test of Radiation Hardness of CMOS Transistors Under Neutron Irradiation

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TEST OF RADIATION HARDNESS OF CMOS TRANSISTORS UNDER NEUTRON IRRADIATION

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ABSTRACT

We have tested 2 micron CMOS test structures from various foundries in the LAMPF Beam stop for radiation damage under prolongued neutron irradiation. The fluxes employed covered the region expected to be encountered at the SSC and led to fluences of up to 10^{14} neutrons/cm^2 in about 500 hrs of running. We show that test structures which have been measured to survive ionizing radiation of the order MRad also survive these high neutron fluences.

The large Hadron Colliders of the future (SSC, LHC) will require high luminosity to achieve their physics goals. This fact, together with the large hadronic cross-section, will result in very high radiation dosage from charged particles and albedo neutrons to detector elements close to the beampipe and the calorimeters. Because of the large multiplicities and particle densities, the number of channels of the read-out will be very large and the electronics have to be integr ted and placed close to the detectors, thus exposing the VLSI read-out to the radiation. Hence, one of the main requirements for SSC/LHC front-end electronics is that it is radiation hard. The SSC Workshop on Radiation Levels in the SSC[1] found that, for example, a silicon tracking device at a radius of 8cm has to survive about 1 MRad and 10^{13} neutrons/cm^2 per year.

We have designed a fast read-out system for Si micro strip-detectors which ultimately will run at the SSC collision rate (60 MHz)[2] and have built 10 MHz prototypes in 2 micron CMOS[3] We are now evaluating rad-hard technologies for

the production of a rad-hard chip for the LPS spectrometer in the ZEUS detector at HERA.

To compare different technologies, we have irradiated various test structures on 2 micron CMOS chips with neutrons in the LAMPF neutron spallation source at Los Alamos National Lab.[4] This source is located in the beam-stop area of the LAMPF 800 MeV proton Linac and thus provides a neutron spectrum similar to the one expected for albedo neutrons in the SSC detectors with a characteristic neutron energy of 1 MeV. The fluxes employed here were between 0.1 to 100 times the ones expected at the SSC.

We have quantified the radiation damage to CMOS transistors by measuring the drain-source current I_{DS} as a function of the gate voltage and determining the shift of the threshold voltage V_{th} as function of dose. The measurements were done *in situ*, providing us with a continuous history of the damage. Figure 1a shows I_{DS} for the non-rad device #2 of Table 1 and Fig. 1b shows I_{DS} for the rad-hard device #7 of Table 1 for different doses. We defined the threshold voltage V_{th} as the gate voltage which produces a drain-source current of $1\mu A$. Figure 2 shows V_{th} as function of the integrated proton current in the Linac for the data shown in Fig 1. The final proton current integral corresponds to a neutron fluence on the chips of about 10^{14} neutrons/cm^2, where the exact number is still being determined from activation foils and will be known at the time of the conference. Table 1 shows threshold voltage shifts ΔV_{th} for different devices and the corresponding estimated fluences: devices #1, #2 and #3 were furnished by MOSIS (MOS Implementation Service) out of non-rad runs done in 1987/1988 by ORBIT and UTMC, devices #4–#7 are rad-hard devices from UTMC

TABLE 1

Device #	Foundry	Transistor type	ΔV_{th} (mV)	Fluence neutrons/cm^2	Remarks
1	ORBIT	n	>600	$\approx 3 \times 10^{11}$	Gate Oxyde :400 Å
2	ORBIT	p	3200	$\approx 3 \times 10^{13}$	Gate Oxyde :400 Å
3	UTMC	n	520	$\approx 10^{14}$	Gate Oxyde :200 Å
4	UTMC	n	45	$\approx 10^{14}$	rad-hard process
5	UTMC	p	100	$\approx 10^{14}$	rad-hard process
6	UTMC	n	30	$\approx 10^{14}$	rad-hard process
7	UTMC	p	>30	$\approx 10^{14}$	rad-hard process

As is evident, the transistors manufactured in non-rad-hard processes (#1 #3), are damaged by the neutron irradiation. This effect could be explained by

the interaction in the gate oxid of heavily ionizing Si atoms which are displaced by the neutrons, as evidenced by the increased hardness of transistors with thinner gate oxid. The radiation-hard transistors from UTMC (#4–#7) have been tested to be rad-hard to several MRad in ionizing radiation[5] and also exhibit good resistance to damage under neutron irradiation. Their performance let us expect that they will offer sufficient radiation resistance for application in the SSC, LHC and HERA. The next phase of our development will be the test of the functionality of read-out chips after irradiation.

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3. J. DeWitt *et al.*, contribution to this Conference.
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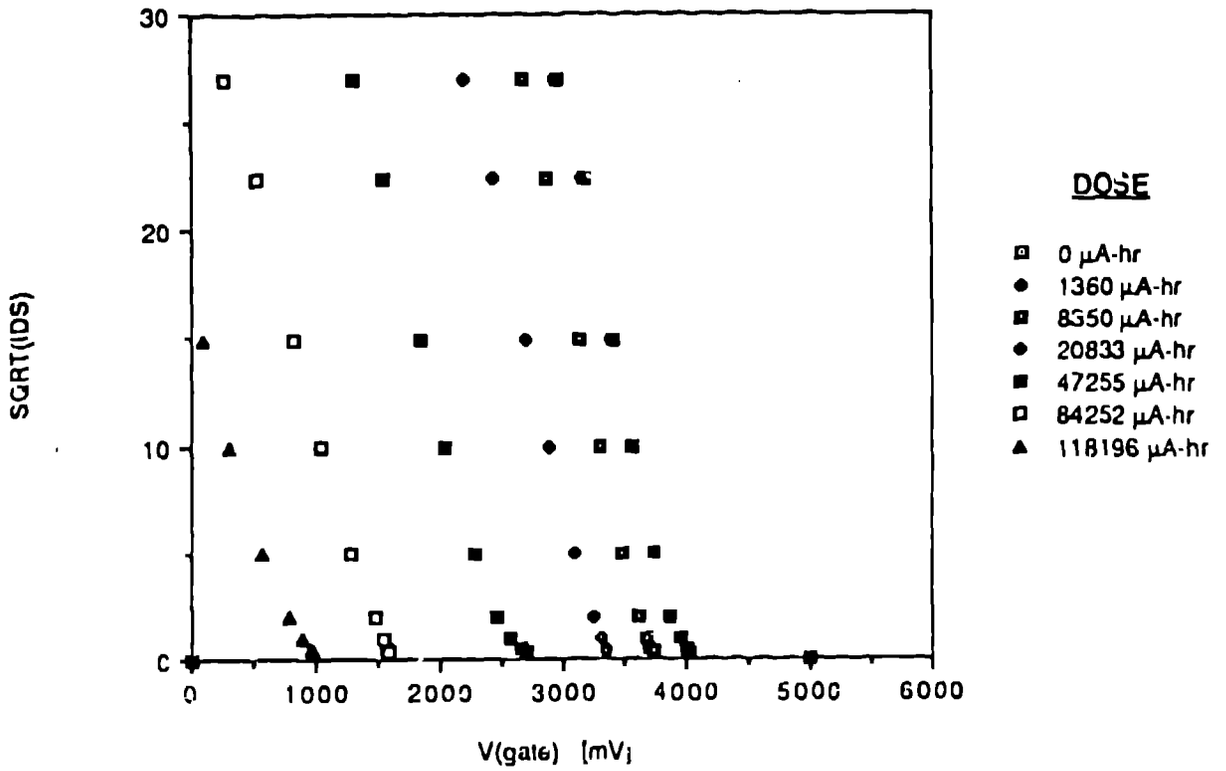

Fig. 1a. Square root of the drain-source current I_{DS} as function of the gate voltage for the non-rad hard p transistor #2 manufactured by ORBIT for different doses.

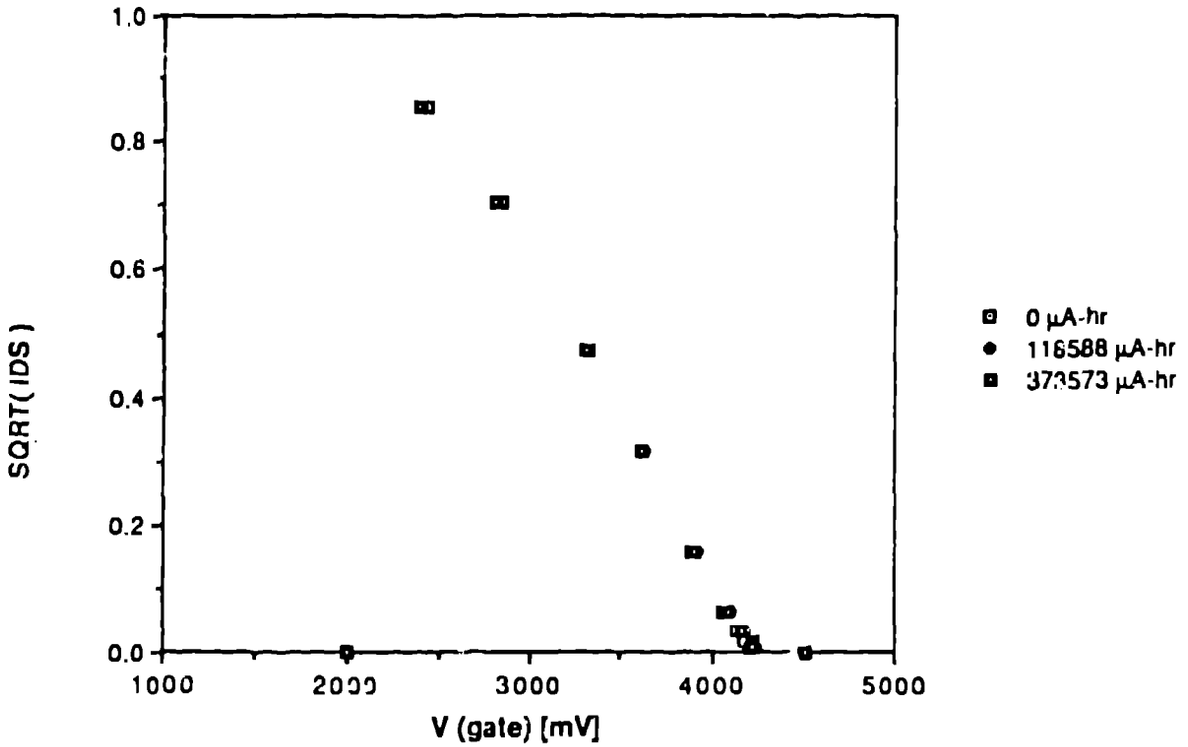

Fig. 1b. Square root of the drain-source current I_{DS} as function of the gate voltage for the rad hard p transistor #7 manufactured by UTMC for different doses.

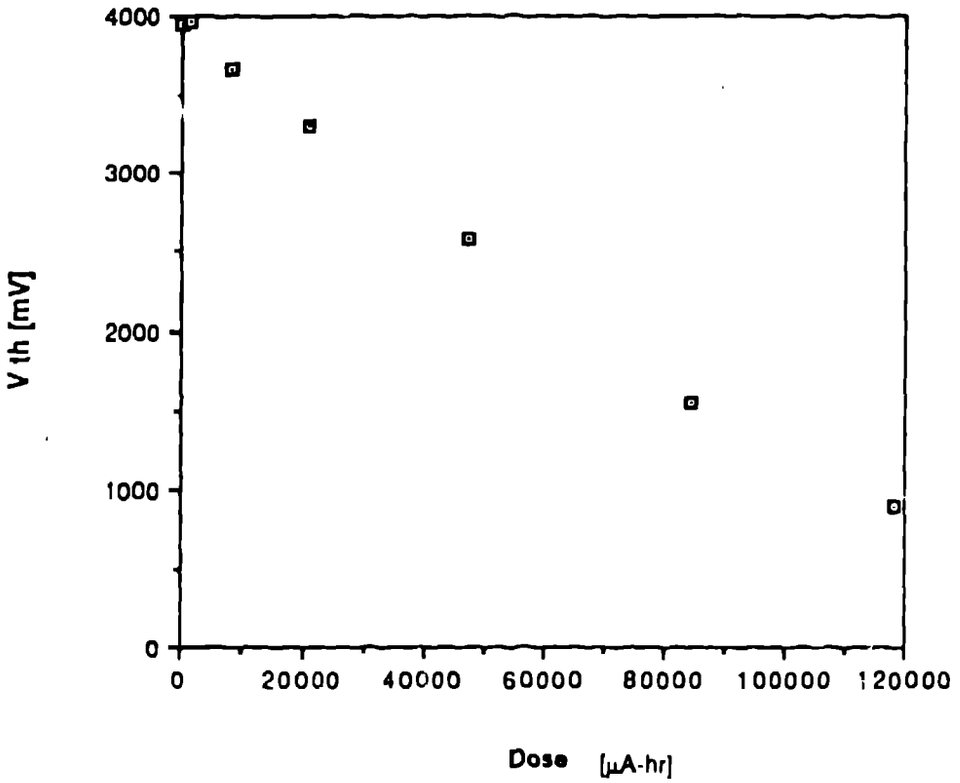

Fig. 2a. Threshold voltage V_{th} vs. integrated proton current for the non-rad hard *p* transistor manufactured by ORBIT.

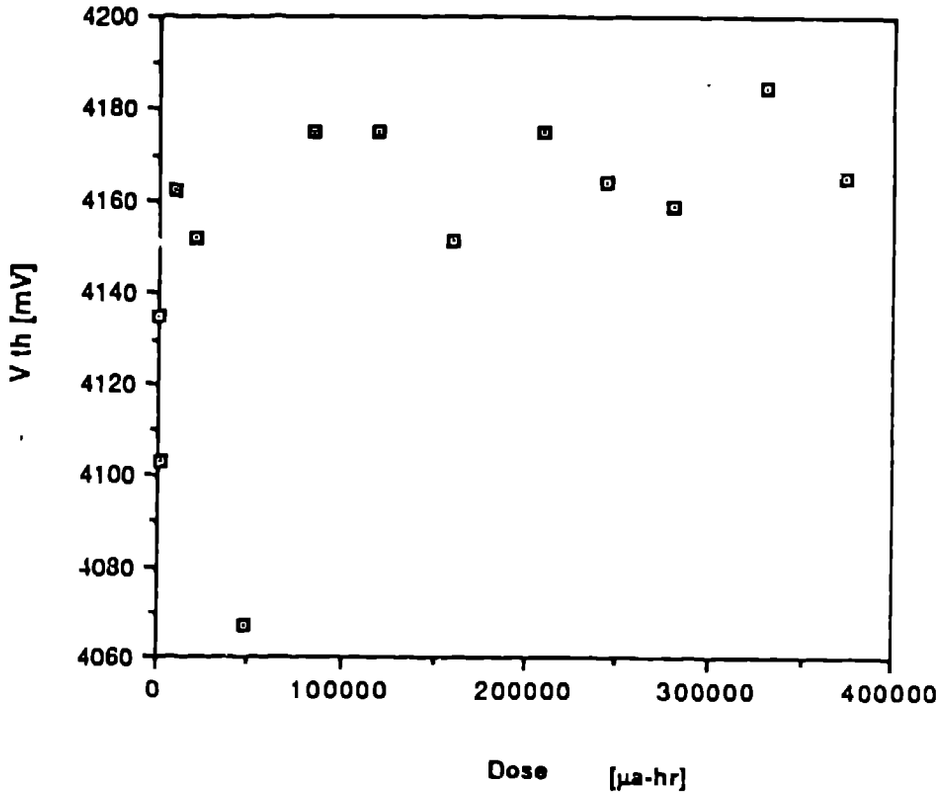

Fig. 2b. Threshold voltage V_{th} *vs.* integrated proton current for the rad hard *p* transistor #7 manufactured by UTMC.